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A low-voltage wide-input CMOS comparator for sensor application using back-gate technique

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Abstract

In this paper, two new analog CMOS comparators (Type-I and Type-II) with low-voltage and wide-input capabilities are proposed. The comparator receives two analog inputs and puts out one digital state to identify the larger (or the smaller) of the input variables, which represents an useful operation in data conversion and sensory signal processing. Without using special fabrication technologies, the supply voltage of the circuit is reduced to 1 V. Due to the utilization of CMOS back-gate technique, the input range of the comparators is greatly improved. The comparators are composed of bulk-driven stage and dynamic latch. By using a CMOS n-well technology, the results of HSPICE simulations indicate that the response time of Type-I circuit is 1 μs under 10 mV identified resolution. Type-II comparator achieves 5 mV identified resolution. The input dynamic ranges of the comparators are approximately rail-to-rail.

Keywords: Comparator; Low-voltage operation; Back gate

1. Introduction

The comparator is an import element in signal processing systems, such as telecommunication interfaces, analog-digital converters, as well as in the sensory circuits. Precision, speed, power consumption, input range, and chip area must be noticed for a comparator design. Since CMOS integrated circuit fabrication is continuously improving, via thinner gate oxides, reduced device size, and so forth, the voltage supply of VLSI circuit in sub-micron technologies must be reduced. Furthermore, portable battery-operation equipments such as biomedical electronics and telecommunication equipments are common applications recently. Thus, design of a low-voltage low-power comparator is an important research. Many high-performance comparators have been proposed (Wu and Wooley, 1988; Yin et al., 1992; Atherton and Simmonds, 1992; Razavi and Wooley, 1992; Laug et al., 1992; Bruccoleri and Cusinato, 1996; Shih et al., 1997; Cusinato et al., 1998; Kotani et al., 1998; Boni et al., 2000). Research work for these comparators has focused on offset cancellation, high-operating speeds, and high-accuracy requirements, yet all of them operate in a supply range of 3–5 V. In open literature, designs of low-voltage comparators are also proposed (Abo and Gray, 1999; Terada et al., 2000; Waltari and Halonen, 2001; Fayomi et al., 2001; Rombouts et al., 2001; Hung and Liu, 2003). However, the reliability, the input range, and the speed of these comparators must be further improved for biosensor's application. Due to the low-voltage requirement, this paper proposes two 1 V wide-input CMOS comparators without using special technologies. Since no extra fabrication mask is required, the fabrication cost is reduced.

2. Circuit design

2.1. CMOS back-gate technique

For a low-voltage VLSI circuit design using a common CMOS fabricated process, one of the major problems is the threshold voltage. Although the CMOS transistor is a four terminals device, the n-well (or n-substrate) terminal is often connected to the positive voltage and the p-well (or p-substrate) terminal is connected to the negative voltage. Using the three-terminal MOS transistor, a commonly used

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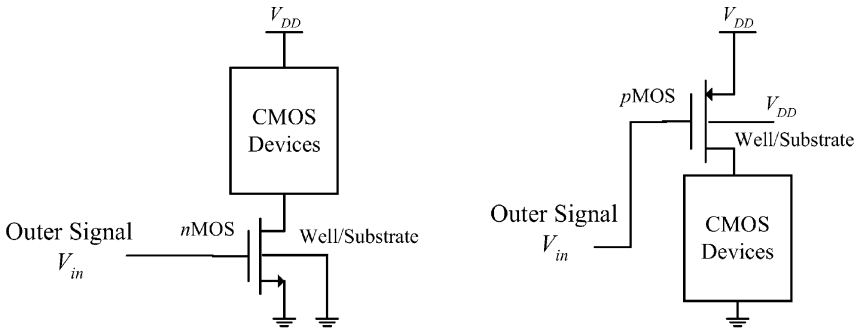

(a) Input range: $V_{in} > V_{tn}$ (b) Input range: $V_{in} < V_{DD} - |V_{tp}|$

Fig. 1. (a) nMOS driven and (b) pMOS driven for sensor signal processing.

schematic for sensor applications is shown in Fig. 1. The sensor signal drives the gate of the MOS transistor. Due to the threshold voltage, the input range is restricted especially for low-supply voltage. In general, a common fabricated process, the threshold voltages of nMOS and pMOS range from 0.5 to 0.85 V. Thus, the input range available is only 15–50% that of the full range when 1 V supply voltage is used, in spite of the fact that nMOS or pMOS is used as input transistor. Due to the weak output level of the sensor's signal, the conventional structures are restricted to apply to process the weak signal. In this paper, the fourth terminal, that is, back-gate (bulk terminal or well terminal) is used as the transistor input to eliminate this limitation. As a first-order approximation, the drain-source current I_{ds} of a MOS transistor working in the saturation region is expressed as

$$|I_{ds}| = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)(|V_{GS}| - |V_t|)^2 \quad \text{and}$$
$$V_t = V_{t0} + \gamma\left(\sqrt{2|\phi_F| - V_{BS}} - \sqrt{2|\phi_F|}\right) \tag{1}$$

where μ is the carrier mobility, C_{ox} the gate oxide capacitance per unit area, W/L the transistor aspect ratio, V_{GS} the gate-source voltage, V_{t0} the zero-bias ($V_{BS} = 0$) threshold voltage, γ the body effect factor, ϕ_F the Fermi potential, and V_{BS} is the bulk-source voltage.

Eq. (1) shows that by increasing the bulk-source reverse voltage, the effective threshold voltage is increased. As a result, the drain-source current is reduced. In contrast, a minimal forward bulk-source voltage results in the drain-source current increasing. Since modifying the bulk voltage varies the effective threshold voltage, the input signal drives the bulk terminal to vary the drain-source current. In this work, the bulk-driven technique is used to design the low-voltage comparators.

2.2. Type-I comparator

Fig. 2 shows the schematic of the comparator cell and the clock waveforms. The supply voltage V_{DD} is 1 V. Input transistors pMOS M_{1p} and M_{2p} are located in the separate n-well, and the n-well terminals are driven by input voltages V_{in1} and V_{in2}, respectively. The dash block of Fig. 2 is a negative voltage generator for biasing M_{1p} and M_{2p}. In general, input transistor with a large device size is required in most of conventional back-gate designs for the larger trans-conductance (g_m) operations. Based on the negative voltage design, the sizes of the input transistors (M_{1p} and M_{2p}) are able to be within a reasonable size. The comparator operates in three phases, a reset phase, a sample phase, and a comparison phase. Referring to the clock waveforms, in the reset phase, transistor M_{cmp} is off, and M_{rst1}, M_{rst2}, M_1, and M_2 are on. The voltage at node z is less than V_{tp} and the voltage at node w is V_{DD}. Thus, the output voltages V_{out1} and V_{out2} are pushed down to zero level to reset the comparator. In the next phase, due to the negative voltage generator, the potential of V_z is boosted negatively to become less than $-|V_{DD}|$. In the meantime, the transistors M_{1p} and M_{2p} reflect the magnitude of the input voltages on nodes x and y. The reflected voltages are sampled at the input of the positive-feedback latch stage. Finally, in the comparison phase, transistor M_{cmp} is turned on to enable the dynamic latch operation. After a time delay t_d, V_{out1} and V_{out2} respond to proper digital states to indicate which input has the larger magnitude. The time delay t_d is approximately equal to

$$t_d \propto \frac{C}{g_m} \tag{2}$$

where C is input node capacitance of the dynamic latch and g_m is the transconductance. The function of the comparator is summarized as

$$V_{out2} = \begin{cases} 1, & \text{when } V_{in1} > V_{in2} \\ 0, & \text{when } V_{in2} > V_{in1} \end{cases} \tag{3}$$

The bulk-driven stage ($M_{1p}/M_1/M_{rst1}$ and $M_{2p}/M_2/M_{rst2}$) is the core of Type-I circuit. The operation of Type-I comparator is sensitive to these devices sizes and the matching property. M_{1p} and M_{2p} determine the magnitude of an initial current. M_1 and M_2 determine the power dissipation and set the proper dc biasing. In order to achieve a wide-input range,

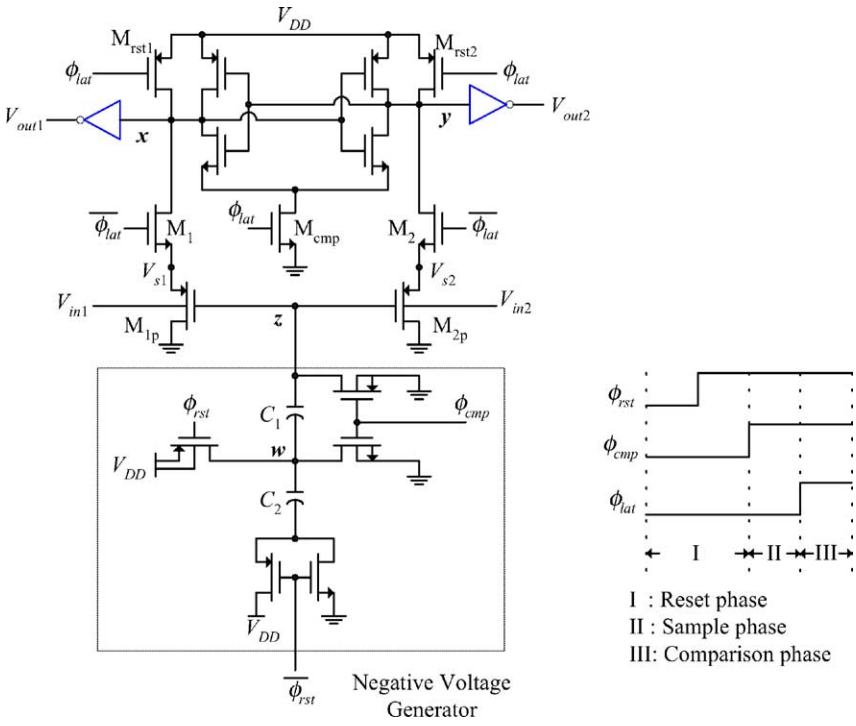

Fig. 2. (a) Schematic diagram and (b) clocks of Type-I comparator.

the voltage levels V_{s1} and V_{s2} must be restricted to prevent p–n junction turn on when input signal is low level. From the latch stage point of view, since the inputs of the latch stage are single ended driven, the precision of the whole circuit is sensitive to noise interference. The noise sources include initial level variance at node *z* (the gates of M_{1p} and M_{2p}), clocks feed-through errors, clocks synchronous of the input stages, and the matching required. As a result, when the comparator is realized by using different technologies, the devices dimensions will be resized. In addition, one important design issue is the biasing levels of nodes *x* and *y*. Since the dynamic latch is implemented by using a common technology, there is a meta-stable region in existence, especially in a low-voltage supply. In this meta-stable region, both nMOS and pMOS transistors in the dynamic latch are turned off; meanwhile, the comparator does not work to identify which one input has larger level. As a result, the device size of the bulk-driven part must be redesigned to adjust the biasing condition when an external supply voltage or fabricated process varies.

2.3. Type-II comparator

The operation of Type-II comparator is similar to Type-I circuit. The comparator is composed of two stages, a bulk-driven stage and an output stage. Fig. 3 shows the schematic of the comparator. A negative voltage generator is designed for M_{1p} and M_{2p} biasing. In order to prevent the source-well junctions of input transistors (M_{1p} and M_{2p}) forward biasing when input voltage is low level, transistors M1 and M2 restrict the V_x and V_y levels. Based on the design, a complementary outputs V_a and V_b in Fig. 3(a) are expressed as

$$V_a = f(i_{SD1} - i_{SD2}) = f(f(V_{in1}) - f(V_{in2})) \quad \text{and}$$
$$V_b = f(i_{SD2} - i_{SD1}) = f(f(V_{in2}) - f(V_{in1})) \qquad (4)$$

According to the levels of V_a and V_b, a positive-feedback output stage shown in Fig. 3(b) generates the proper logic states to indicate which input has a larger magnitude. The comparator operates in two phases: reset phase and comparison phase. In reset phase, the output stage shown in Fig. 3(b) is disabled to reset the comparator. In comparison phase, according to V_a and V_b, the output stage regenerates the output levels to a proper logic state. Using clock-pumping technique, Fig. 3(c) shows a new two-stage negative voltage generator to bias the comparator. Each stage is composed of two capacitors and two pMOS transistors. Capacitors, transistors M_p, and clock ϕ_{clk} constitute a charge-pump mechanism to pump a negative level. Transistors M_{po1} and M_{po2} operate as output switches. Furthermore, in order to reduce clock complexity, an on chip clock generator is designed. Fig. 4 shows the functional block. Symbol D-latch represents a D-type latch, in which symbol *D*, *Q*, and $\bar{Q}$ represent the data input, data output, and complementary output of D-type latch stage, respectively. By using a D-type latch, NOR gates, and some inverters, the desired internal clocks are generated. Thus, a single external clock is arrived to reduce the external clock complexity.

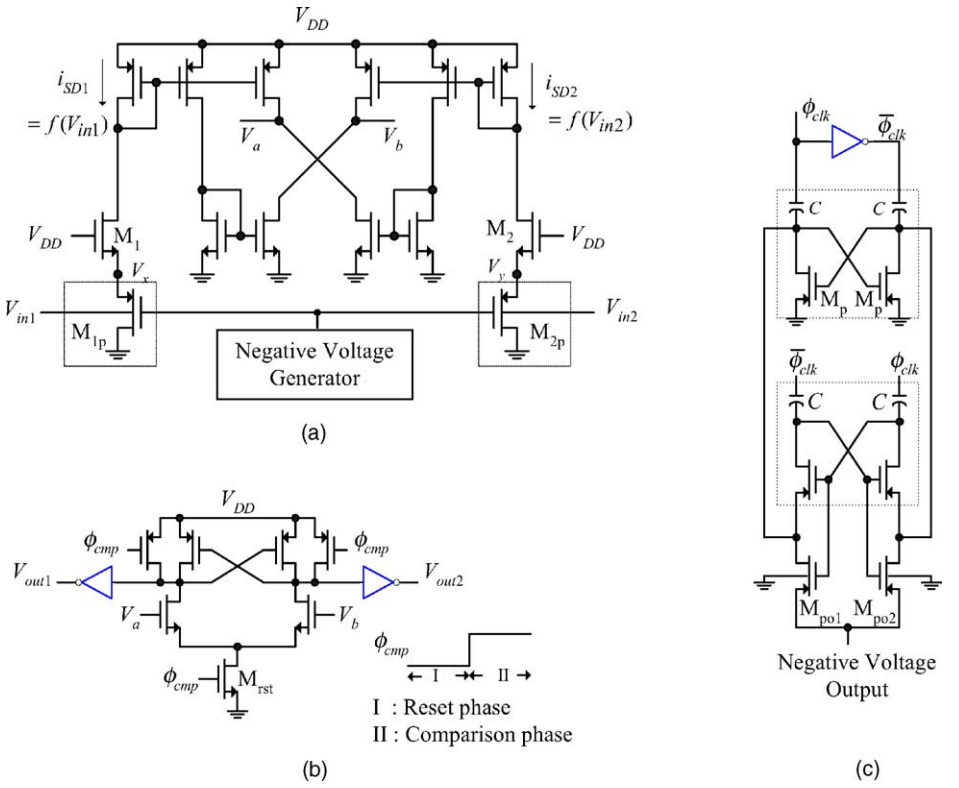

Fig. 3. (a) Preamplifier, (b) output stage, and (c) negative voltage generator of Type-II comparator.

In contrast to Type-I comparator, Type-II circuit contains higher noise immunity than Type-I. The two inputs of the latch stage are complementary, that is, $V_a = f(f(V_{in1}) - f(V_{in2}))$ and $V_b = f(f(V_{in2}) - f(V_{in1}))$. The common-mode noises at these input terminals are almost eliminated. Focusing on Fig. 3, the output levels of the bulk-driven stage, V_a and V_b, these levels drive the gates of transistors of succeeding output stage. Thus, the levels of V_a and V_b, must be larger than one threshold voltage. Depending on the magnitude of negative voltage and the speed requirement, the device sizes of M_{1p} and M_{2p} must be adjusted to hold a reasonable transconductance.

3. Simulation results

3.1. Type-I: simulation results

By using a 0.5-μm double-poly double-metal n-well CMOS technology, an experimental comparator was designed. With a V_{DD} of 1 V, various input voltages were applied to test the comparator's precision and input range. The inputs, at each 1 μs per voltage level, were:

$$V_{in1}(t) = (0.00\,V, 0.11\,V, 0.30\,V, 0.51\,V, 0.70\,V, 0.91\,V, 0.99\,V)$$

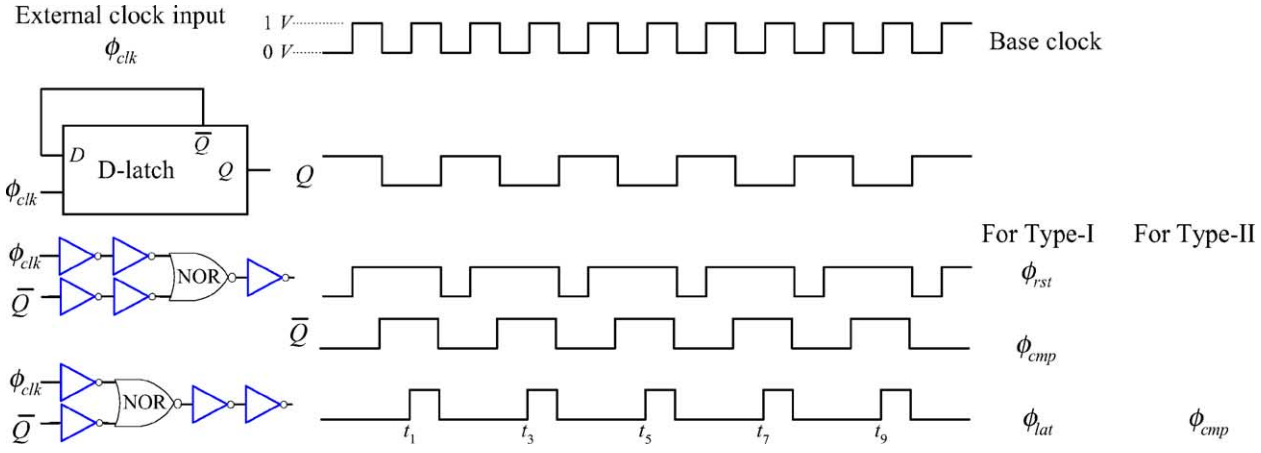

Fig. 4. On-chip clocks generator.

and

$$V_{\text{in2}}(t) = (0.01\,\text{V}, 0.10\,\text{V}, 0.31\,\text{V}, 0.50\,\text{V}, 0.71\,\text{V}, 0.90\,\text{V}, 1.00\,\text{V}).$$

The clock high was 1 V (V_{DD}). The periods of the clocks ϕ_{rst}, ϕ_{cmp}, and ϕ_{lat} were 1 μs with a 75, 50, and 25% duty cycles, respectively. The capacitances C_1 and C_2 were 1.0 pF. The results of HSPICE simulation show that each comparison was finished within 1 μs, and the outputs of the comparator exactly indicate which input with the larger magnitude. Inputting two tri-angular waveforms to the comparator gave a dynamic response. The magnitude of one of the inputs is always smaller than the other input when $0 < t < 10\,\mu\text{s}$, that is, $V_{\text{in2}}(t) = V_{\text{in1}}(t) - 0.01$. The input setting, however, is $V_{\text{in2}}(t) = V_{\text{in1}}(t) + 0.01$ when $10\,\mu\text{s} < t < 20\,\mu\text{s}$. Observing the simulated results, the comparator functions well in this dynamic response test.

3.2. Type-II: simulation results

An experimental circuit was designed by using a 0.25-μm n-well CMOS technology. The inputs, at each 1-μs per voltage level, were:

$$V_{\text{in1}}(t) = (0.005\,\text{V}, 0.100\,\text{V}, 0.205\,\text{V}, 0.300\,\text{V}, 0.505\,\text{V}, 0.800\,\text{V}, 1.000\,\text{V})$$

and

$$V_{\text{in2}}(t) = (0.000\,\text{V}, 0.105\,\text{V}, 0.200\,\text{V}, 0.305\,\text{V}, 0.500\,\text{V}, 0.805\,\text{V}, 0.995\,\text{V}).$$

Clock high was 1 V (V_{DD}). The period of clock ϕ_{cmp} was 1 μs with a 75% duty cycle. The capacitances C used in the negative generator were 2.0 pF. Fig. 5 shows the results of the HSPICE simulation, with output responses V_{out1} and V_{out2} shown in top trace and bottom trace, respectively. In Fig. 5, each comparison was finished within 1 μs, and the outputs of the comparator exactly indicated which input with the larger magnitude. Furthermore, inputting two tri-angle waveforms, the dynamic response of the comparator was also shown in Fig. 5(b). The magnitude of one of the inputs is always smaller than the other input when $0 < t < 210\,\mu\text{s}$, that is, $V_{\text{in2}}(t) = V_{\text{in1}}(t) - 0.005$. The input setting, however, is $V_{\text{in2}}(t) = V_{\text{in1}}(t) + 0.005$ when $210\,\mu\text{s} < t < 420\,\mu\text{s}$. Fig. 5(b) shows the comparator functions successfully in the dynamic test.

In order to verify Type-II comparator with a high stability, many non-ideal factors such as device dimension variation, transistor threshold variation, supply voltage variation, and clocks skew effects were simulated. When the dimension and threshold voltage of transistors are varied from −10% to +10% of nominal values, by simulation the comparator still works successfully. In an integrated circuit, substrate noise degrades the quality of a supply voltage, especially for a mixed-mode design. In this experiment design, when the supply voltage varies from 0.7 V to 1.3 V, the results of simulation indicate the comparator functional. This means that the supply voltage of the comparator allows a tolerance in ±30% variation of V_{DD}. In addition, the comparator also allows clock skew within 200 ns.

3.3. Chip implementation and discussion

Capacitors in the experimental chip were implemented by two layers of polysilicon. The input transistors (M_{1p} and M_{2p}) used in the comparators are located in the separated n-well. A guard ring technique is used to inhibit substrate noise. The active area of Type-I comparator (including the capacitors C_1 and C_2) is 100 μm × 95 μm, and the chip area of Type II is 100 μm × 240 μm. In this design, the device size of Type-II for the comparator's performance is not an important issue. The major part of the layout area is the capacitors implementation. The layout area can be greatly reduced when the technology parameters modification relates

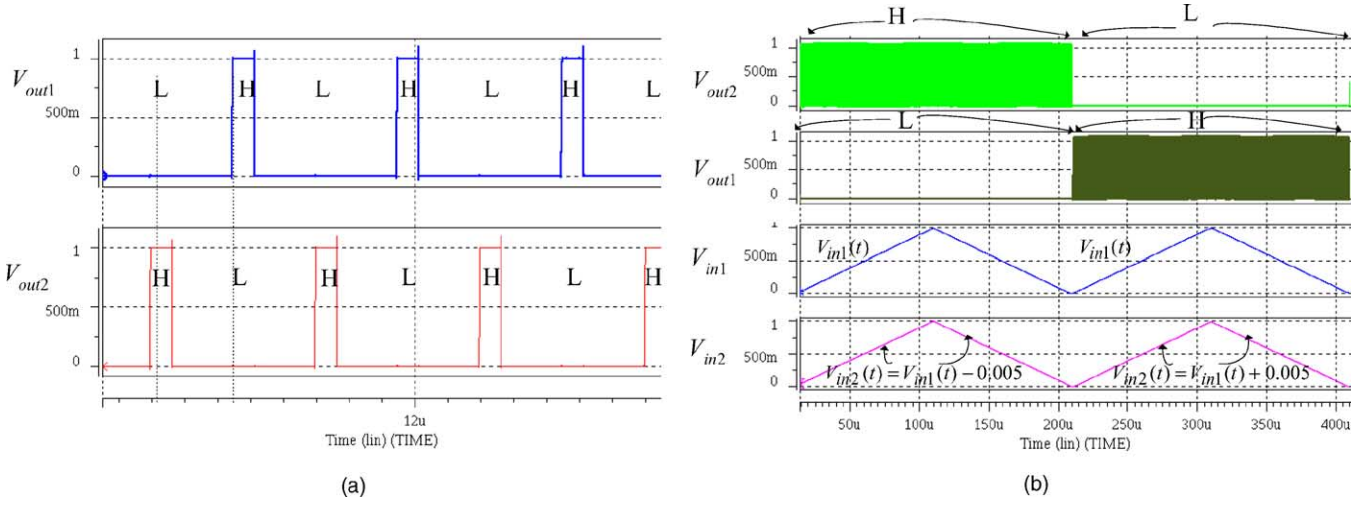

Fig. 5. Simulated results of Type-II comparator.

Table 1
Summary of the comparators

	Low-voltage comparator	
	Type-I	Type-II
Technology	0.5-μm CMOS n-well $V_{tn} = 0.74$ V; $V_{tp} = 0.85$ V	0.25-μm CMOS n-well $V_{tn} = 0.48$ V; $V_{tp} = 0.60$ V
Input variable	Voltage signal	
Input range	Nearly rail-to-rail	
Response time	1 μs (simulation)	
Precision	10 mV (simulation)	5 mV (simulation)
Supply voltage	1 V	
Circuit architecture	Back-gate driven and positive-feedback latch	
Power dissipation	0.95 nW @ 1.0 V (static) 7.3 μW @ 10 V (dynamic average)	9.0 μW @ 1.0 V (static) 12 μW @ 1.0 V (dynamic average)
Comparator chip area	100 μm × 95 μm	100 μm × 240 μm

via process improvement. Fortunately, when multiple comparators are required for application requirement, the capacitor is shared among many comparator cells. As a result, when multi-comparator cells are required, the sharing of a negative voltage generator will effectively reduce the layout area.

Design of a biasing optimization for the low-voltage analog CMOS bulk-driven circuit is not an easy work. The performance of the comparator is varied when the biased point shifts due to process variation and supply voltage modification. After the observation of the corners simulations (FF FS, SF, SS), Type-II comparator functionally works, and little function of Type-I comparator is varied due to this parameter variation. In order to obtain the maximum speed and precision, transistor size of Type-I circuit has to be slightly tuned when a process variation However, Type-I comparator with less circuit complexity is functional when the precision and speed requirements are down grade.

Table 1 summarizes the characteristics of the circuits. The advantages of the proposed circuits are the ability to use a low-voltage supply, the small power consumption, and the ability to accept a wide input range without using a special VLSI fabricated process. Table 2 shows the characteristics of the circuits comparing with other low-voltage comparators in open literature. The precision and the wide-input properties in this research are noticeable. A possible drawback of the comparators is the chip area consideration.

3.4. Characteristics of Type-I and Type-II comparators

Both Type-I and Type-II comparators work at 1 V supply within 1 μs response time. Type-I comparator has smaller power dissipation, less circuit complexity, and smaller chip area than Type-II comparator. However, the performance of Type-I comparator is sensitive to device size. Based on the complementary design of Type-II comparator, Type-II has a high stability against many non-ideal effects. From the stable point of view, performance of Type-II is better than Type-I. The other one difference between the two comparators is initial time. Since the negative voltage generator used in Type-II comparator requires an initial time to generate a proper negative level, the operation of Type-II comparator must have a waiting time; the initial time of Type-I, however, is not needed.

Since the bulk-driven stage is the core of the comparators, a brief analysis on the bulk-driven stage for frequency response is considered. Based on a MOSFET high-frequency equivalent circuit and Miller's theorem, a 3-dB frequency of the bulk-driven stage is obtained. The 3-dB frequency is approximately expressed as

$$f_{3\,\mathrm{dB}} \cong \frac{1}{2\pi R_s C_{\mathrm{in}}} \quad \text{and}$$

$$C_{\mathrm{in}} = C_{\mathrm{gb1}} + C_{\mathrm{db1}} + \left(1 + \frac{g_{\mathrm{mb1}}}{g_{\mathrm{m1}} + g_{\mathrm{m2}} + g_{\mathrm{mb1}}}\right) C_{\mathrm{sb1}}$$

Table 2
Low-voltage comparator characteristics comparisons

Circuit	Abo and Gray (1999)	Terada et al. (2000)	Waltari and Halonen (2001)	Fayomi et al. (2001)	Rombouts et al. (2001)	Hung and Liu (2003)	This Work
Supply voltage (V)	1.5	1	1	1	1.2	1	1
Precision	Less 200 mV error	15 mV	150 mV	0.122 mV (simulated)	N/A	10 mV	Type-I: 10 mV; Type-II: 5 mV (simulated)
Response time	4 ns decision	10 ns	5 MHz clock rate	16.67 MHz clock (simulated)	256 kHz clock	4 μs	1 μs (simulated)

where R_s is the resistance of input signal, C_{gb1}, C_{db1}, and C_{sb1} the gate-bulk, drain-bulk, and source-bulk capacitances of transistor M_{1p} or M_{2p}, respectively, g_{m1} and g_{mb1} the transconductance of transistor M_{1p} or M_{2p}, g_{m2} the transconductance of transistor M_1 or M_2.

Due to the low-voltage operation, many factors degrade circuit performance such as noise interference (internal and external), small SNR, driving capability decrease, and parasitic capacitances. In order to relief these effects, many techniques are adopted such as (1) using pMOS as input transistor reduces the device noise; (2) bulk-driven part of the circuit is surrounded by guard ring to reduce the substrate noise; (3) extra output buffer is needed to increase driving capability when internal signal drives the chip output pad.

The behavior of the comparators is analogue inputs and digital outputs. Output buffers are utilized in this design. The output digital states through the output buffers are measured by using a high-impedance oscilloscope or a digital meter. By using a high-precision power supplier (with the precision of mV order), two analog input levels are set for the precision test. In practical way, a low-noise preamplifier embedded into the comparators will improve the performance and will enhance the noise immunity.

4. Conclusion

Without using a special fabrication technology, the design of two wide-input comparators working at a 1 V supply voltage is presented, which uses back-gate and clock-boosted techniques. By simulation, Type-I and Type-II comparators are able to distinguish a 10 and 5 mV difference within 1 μs, respectively. These low-voltage wide-range comparators are suitable for small signal processing. Importantly, the comparator is easily integrated within low-voltage system-on-chip (SoC) applications.

Acknowledgements

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